REMARKS

Reconsideration is respectfully requested.

This Amendment, Claims 1, 11 and 13 have been amended to remove the word "substantially" so as overcome the reference under 35 U.SC. §112, second paragraph. Claims 1 and 11 have been further amended to recite further distinguishing features not shown in the references of record.

Claims 1, 11 and 13 were rejected under USC 103(a) as being unpatentable over Grube et al. in view of Mones et al. The Grube et al. reference, Fig. 6A, discloses the metal column (620) and the insulating layer (612) in the vicinity of the metal column (620). The metal column (620) has nothing to relate it with the insulating layer (612). That is, the insulating layer (612) does not surround the metal column (620) for protection and the height of the metal column (620) is not at the same level as that of the insulating layer (612). The metal column (620) of the Grube et al. reference may be damaged or disengaged from the conductive layer (610) if a side force is applied to the side the metal column.

The part indicated by the reference number 16 in the Mones et al. reference is a bump, which is connected to a mounting board by being melted or by forming a eutectic alloy. On the other hand, the metal column according to the present invention has a top surface which serves as a pad (connection service) to be connected to a semiconductor element, and the metal column itself does not melt nor form a eutectic alloy when connected to the semiconductor element.

In the structure of the present invention, when a solder bump of a semi-conductor element is subjected to a solder-reflow process, the melted solder bump is prevented from

flowing down along the circumferential side surface of the resin film 206. The resin film 206 is formed by a material different from the material of the metal column 208, and thus, the properties of the top surface 206a of the resin film 206 are different from the properties of the top surface 208a of the meal column 208. Accordingly, the melted solder on the top surface 208a of the metal column 208 does not spread to the top surface 206 of the resin film 206, which results in prevention of the melted solder flowing along the side surface of the resin film. Thus, the melted solder is prevented from being filled in the gap between the resin film 206 and the insulating layer 210 which may prevent a stress relaxation effect of the metal column and the gap around the metal column.

Additionally, since the solder does not flow and stay on the top surface of the metal column, there is no need to provide an excessive amount of solder, which prevents the bump from being excessively large. Thus, a semi-conductor element having high-density bumps can be connected.

Claims 1 and 11 have been amended to more clearly recite these features, not shown or described by either of the relied upon references.

The Mones et al. reference does not disclose such a structure having the above-mentioned effects.

The Grube et al. reference merely discloses a wire having a central portion covered by an insulating material as shown in FIG. 6A. Thus, the melted solder may flow along the side surface of the wire. Additionally, there is a description that the diameter of the wire is 0.7-2.0 mil. This means that the top of the wire exposed from the insulating material is very small and cannot form a pad for connection.

With respect to the disapproval of the earlier submitted drawing corrections, Applicants again submit the drawing corrections showing the extension of the lead line for element 107 to indicate the correct illustrated feature. The drawing correction is sent by mail (courtesy copy attached hereto), so that the red line markings are clearly shown.

For the above reasons, it is considered that the claims, as amended, find support in the parent application specification as filed, and that the combination of elements recited in the pending claims, as amended, distinguish over the references of record. Accordingly, an indication of allowable subject matter is earnestly solicited.

Respectfully submitted,

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MARKED UP COPY OF CLAIMS

1. (Twice Amended) A multilayer interconnection substrate comprising:

an uppermost interconnection layer having a plurality of terminal pads formed at positions corresponding to a plurality of external connection terminals provided on a semiconductor element which is to be mounted on said multilayer interconnection substrate;

a metal column formed on each of said terminal pads, and having a top surface;

a resin film covering a side surface of said metal column, and having a top surface; and

an insulting layer [fumed] formed on said uppermost interconnection layer so that a gap is formed between the insulating layer and an outer peripheral surface of said resin film, wherein an upper end surface of each metal column is [substantially] at the same height as an upper surface of the insulating layer,

the top surface of the metal column and the top surface of the resin film covering the side surface of the metal column are formed at the same level of height; and

the top surface of the metal column is surrounded by and exposed on the resin film so that the top surface of the resin film forms a pad for connection with a semi-conductor element.

11. (Twice Amended) A semiconductor [torn] device comprising:

a multilayer interconnection substrate which comprises an uppermost interconnection layer having a plurality of terminal pads formed at positions corresponding to a plurality of external connection terminals provided on a semiconductor element which is to be mounted on said multilayer interconnection substrate; a metal column formed on each of said terminal pads and having a top surface; a resin film covering a side surface of said metal column and

having a top surface; and an insulating layer formed on said uppermost interconnection layer so that a gap is formed between the insulating layer and an outer peripheral surface of said resin film, wherein an upper end surface of each metal column is [substantially] at the same height as an upper surface of the insulating layer,

the top surface of the metal column and the top surface of the resin film covering the side surface of the metal column are formed at the same level of height; and

the top surface of the metal column is surrounded by and exposed on the resin film so that the top surface of the resin film forms a pad for connection with a semi-conductor element.

13. (Twice Amended) [a] A semiconductor device comprising:

a multilayer interconnection substrate manufactured by forming a plurality of terminal pads in an uppermost interconnection layer; forming an insulating layer on said uppermost interconnection layer; forming openings in said insulating layer, the openings located at positions corresponding to said terminal pads; filling each of said openings with metal particles; forming a metal column in each of said openings by heating said metal particles at a temperature which melts said metal particles so as to define a metal column top surface; and removing a part of said insulating layer near but not adjacent to a peripheral side of said metal column, while leaving a part of said insulating layer adjacent to said peripheral side of said metal column, so that a gap is formed around but not adjacent to said peripheral side of said metal column, wherein [an upper end] the top surface of each metal column is [substantially] at the same height as an upper surface of the insulating layer.